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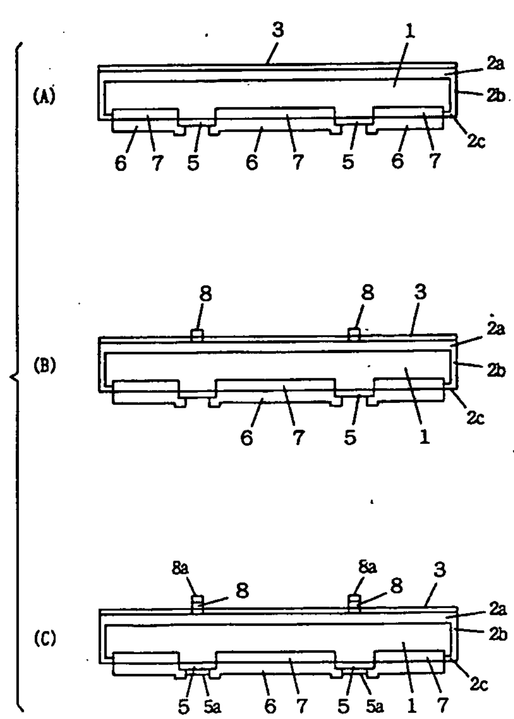
(54) Solar cell and a method of manufacturing thereof.

(57) A solar cell includes a first n type layer (2a) formed on the upper surface of a p type silicon substrate (1), a p type layer (7) formed on the back surface of the substrate (1) and having an impurity concentration higher than that of the substrate (1), and a second n type layer (2b, 2c, 2d) formed at least on the side face of the substrate (1) so as to connect the first n type layer (2a) and the p type layer (7). The second n type layer (2b, 2c, 2d) has an impurity concentration lower than that of the first n type layer (2a) around the region in contact with the p type layer (7).

FIG. 4



BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a solar cell and a method of manufacturing the same, and more particularly, to improvement of a solar cell used in a solar cell module including a plurality of series-connected solar cells and a method of manufacturing the same.

Description of the Background Art

Figs. 19 and 20 show a light receiving surface (also referred to as "front plane") and a back surface of a conventional solar cell. A solar cell 10 includes a semiconductor substrate 1. The front plane of substrate 1 is covered with an anti-reflection film 3. A comb-like front silver electrode is formed on anti-reflection film 3. The front silver electrode is covered with a solder layer 8a. A major portion of the back surface of solar cell 10 is covered with an aluminum electrode 6. Back silver electrodes are formed at a plurality of local regions in the region of aluminum electrode 6. The back silver electrodes are covered with a solder layer 5a.

Figs. 21 and 22 illustrate a method of manufacturing the solar cell shown in Figs. 19 and 20. For the sake of simplification, the dimension between various elements shown in the drawings are not drawn to scale.

It is to be noted that Fig. 21(A) to (D) and Fig. 22(A) to (D) show sequential steps of one manufacturing process.

Referring to Fig. 21(A), a semiconductor substrate 1 is prepared having, for example, a diameter of 100 mm, and a thickness of 0.4 mm. P type semiconductor substrate 1 generally has an impurity concentration in the range of $3x10^{15}$ to $4x10^{16}$ cm^{-3}. A silicon substrate 1 having a main surface of (100) is generally used. Preferably, the light receiving surface of silicon substrate 1 is formed in a pyramid-like concave and convex manner (referred to as "texture surface") as in the circle showing an enlarged portion thereof for the purpose of reducing light reflection. Such a texture surface is formed by treating silicon substrate 1 for 20 to 30 minutes at a temperature in the range of 80 °C to 90 °C while adding isopropyl alcohol in a solution including several % of NaOH.

Referring to Fig. 21(B), an n^+ layer 2 having a thickness of approximately 0.4 µm, for example, is formed all over the surface of silicon substrate 1. n^+ layer 2 can be formed by applying a diffusion process for 45 minutes at 900 °C in an ambient including $POCl_3$ gas, for example. Here, a phosphorus glass film (not shown) is produced on the surface of n^+ layer 2 which is not required. This phosphorus glass film can be removed by dipping the same in a solution including 10 % of HF for one minute.

Referring to Fig. 21(C), an anti-reflection film 3 such as of titanium oxide or silicon oxide is formed by evaporation or CVD on the light receiving surface of substrate 1. Anti-reflection film 3 is formed to a thickness of 70 to 80 nm. The presence of an n^+ layer 2 all over surface of silicon substrate 1 causes shorting between the negative voltage (n side) and the positive electrode (p side) of the solar cell, so that favorable electrical characteristics cannot be obtained. It is therefore necessary to remove n^+ layer 2 at least from the back surface of silicon substrate 1.

Referring to Fig. 21(D), an acid resistant resist 4 is applied on anti-reflection film 3 by screen printing to be dried. Then, an etching step is applied using a mixture of hydrofluoric acid and nitric acid (HF : HNO_3 = 1 : 3), whereby n^+ layer 2 is removed from the side face and back surface of substrate 1.

Then, resist layer 4 is removed using a solvent such as toluene or xylene as shown in Fig. 22(A). Referring to Fig. 22(B), paste 5 including silver and paste 6 including aluminum are printed at a predetermined pattern to be dried. Substrate 1 is subjected to a thermal treatment at 700 °C to 800 °C, whereby a back silver electrode 5 having a thickness of approximately 20 µm and a back aluminum electrode 6 having a thickness of approximately 50 µm are baked. Here, aluminum and silicon are alloyed, whereby a p^+ layer 7 is formed on aluminum electrode 6. p^+ layer 7 has a thickness of approximately 5 µm to induce a BSF (Back Surface Field) effect.

Referring to Fig. 22(C), paste 8 including silver is printed at a predetermined pattern on anti-reflection film 3 to be dried. Then, a thermal treatment is applied to substrate 1 at a temperature in the range of 600 °C - 700 °C, whereby a front silver electrode 8 having a thickness of approximately 20 µm is baked. Here, the silver paste includes glass frit, and front silver electrode 8 forms an ohmic contact with n^+ layer 2 through anti-reflection 3.

Referring to Fig. 22(D), solder layers 5a and 8a having a thickness of approximately 20 µm are formed on the surfaces of back silver electrode 5 and front silver electrode 8, respectively. Thus, a solar cell 10 is completed. The structure shown in Fig. 22(D) corresponds to the structure of Fig. 20 taken along line 24H - 24H.

Although the above description is made of an n^+ layer 2 formed by diffusion using $POCl_3$ gas, an n^+ layer can be formed on a light receiving surface by applying a dopant solution including alkyl silicate, alcohol, carboxylic acid, etc. and phosphorus pentaoxide as a diffusion source on the

light receiving surface of the silicon substrate by a spin coater, which is then subjected to a diffusion thermal treatment. However, this known method results in formation of an n layer also at the back surface and side face of the silicon substrate due to automatic doping caused by out-diffusion from the applied dopant agent. Therefore, this n layer must be removed as in the step shown in Fig. 21-(D) by a resist printing method.

The above-described conventional method of manufacturing a solar cell requires various steps such as a resist printing method to remove unrequired regions of the n type layer, an etching step, and a resist removal step. Therefore, the manufacturing process of a solar cell was expensive.

Furthermore, a conventional solar cell manufactured as described above had problems set forth in the following.

A solar cell is seldom used in a unitary fashion, and a solar cell module is generally used in which a plurality of solar cells are connected in series as shown in Fig. 23(A).

Fig. 23(A) shows the top plane view of a solar cell module including 36 solar cells 10 connected in series. A solar cell 10 is connected to an adjacent solar cell 10 in series by an interconnector 11.

Fig. 23(B) shows a cross section structure of the solar cell module of Fig. 23(A) taken along line 23B - 23B. The solar cell module includes a support plate 12 of transparent tempered glass. Solar cells 10 connected in series by interconnectors 11 are imbedded within an EVA resin layer 13. A white weather resistant film 14 covers the bottom surface of EVA resin layer 13.

Fig. 23(C) is an equivalent circuit diagram of a solar cell module having a plurality of solar cells connected in series. In (C), the small arrows represent light entering a solar cell, and the long arrow I represents the direction of the output current of the solar cell module.

When a solar cell module is actually used, a portion thereof may be shadowed. More specifically, the shadow of a tree, a building, or electric wires is cast on the solar cell module. There is also a possibility of the solar cell module being shadowed by droppings of birds or dust adhered to the surface thereof.

In a mode where a short-circuit is established across solar cells at both ends of the solar cell module, voltage generated from a solar cell which is not shadowed is applied to a solar cell which is shadowed as a reverse bias voltage. In such a shadowed solar cell, power caused by current according to the reverse bias voltage generates heat to be consumed. When this reverse bias voltage exceeds the peak inverse voltage of the solar cell, short-circuit breakdown occurs in that solar cell, whereby the output characteristics of the entire solar cell module is degraded significantly. The rise in temperature and short-circuit breakdown of a shadowed solar cell depends upon the reverse direction properties of a solar cell. It is preferable to facilitate current flow in the reverse direction of a solar cell in order to reduce such phenomenon.

In a conventional solar cell as shown in Fig. 22-(D), complete isolation is achieved by a pn junction between the positive electrode side and the negative electrode side. Therefore, the forward direction properties of the solar cell is favorable so that high conversion efficiency can be obtained. However, current does not easily flow in the reverse direction.

Fig. 24 shows the current voltage (I-V) characteristics of such a solar cell in a qualitative manner. The voltage V is plotted along the abscissa, and the current I is plotted along the ordinate. Curve 24A shows the I-V characteristics of a solar cell illuminated with light, and curve 24B shows the same in a solar cell attaining a darkened state. It is appreciated that reverse direction current cannot easily flow in a solar cell as shown in Fig. 22(A) attaining a darkened state.

Fig. 25 shows an equivalent circuit diagram of a solar cell. It is considered that a solar cell includes parallel resistance and serial resistance. More specifically, it is expected that a solar cell having the I-V characteristics as shown in Fig. 24 has great parallel resistance. It is to be noted that the parallel resistance and serial resistance are not shown in the equivalent circuit diagram of Fig. 23-(C).

Fig. 26 is a graph showing the influence of a shadow in a solar cell module including 36 solar cells, each having a diameter of 100 mm, and parallel resistance of 20 kΩ/cm^2. The output voltage of the solar cell module is plotted along the abscissa, and the output current is plotted along the ordinate. The curve representing 100 % shows the I-V characteristics of a solar cell module in which one light receiving surface of a solar cell is entirely shadowed out of the 36 solar cells. Similarly, the various % numerics corresponding to respective curves represent the rate of the shadowed area formed on one solar cell out of the 36 solar cells. It is appreciated from Fig. 26 that the entire output of a solar cell module is extremely reduced as the area of a shadow formed in one solar cell increases when each solar cell has great parallel resistance.

Fig. 27 shows the result of a simulation in assessing the power consumption of one shadowed solar cell in a solar cell module where 32 solar cells including parallel resistance of 20 kΩ/cm^2 are connected in series. In (A), curve 27B shows the I-V characteristics of one solar cell in which 20 % of the light receiving area is shadowed. Curve 27A

shows the I-V characteristics of the remaining 31 solar cells connected in series. Curve 27C shows the I-V characteristics obtained by combining curves 27A and 27B. The area of the hatched region corresponds to power consumed by the one shadowed solar cell.

Referring to Fig. 27(B), curve 27D shows the I-V characteristics of one solar cell in which 70 % of the light receiving area is shadowed. Curve 27(E) shows the I-V characteristics obtained by combining curves 27A and 27D. By comparing the area of the hatched region between (A) and (B) in Fig. 27, it is appreciated that the power expended by a shadowed solar cell having a shadowed light receiving area of 70 % is lower than that having a shadowed light receiving area of 20 %.

Fig. 28 is similar to Fig. 27 provided that each solar cell has parallel resistance of 1 kΩ/cm^2. Referring to Fig. 28(A), curve 28B shows the I-V characteristics of one solar cell in which 20 % of the light receiving area is shadowed. Curve 28A shows the I-V characteristics of the remaining 31 solar cells. Curve 28C shows the I-V characteristics obtained by combining curves 28A and 28B. Referring to Fig. 28(B), curve 28D shows the I-V characteristics of one solar cell in which 70 % of the light receiving area is shadowed. Curve 28E shows the I-V characteristics obtained by combining curves 28A and 28D. It is appreciated by comparing the area of the hatched regions between (A) and (B) in Fig. 28 that power expended by one shadowed solar cell having a shadowed light receiving area of 70 % is greater than that having a light receiving area of 20 %, contrary to Fig. 27.

Fig. 29 is a graph showing a result of a wider range of such a simulation shown in Figs. 27 and 28. In the present graph, the ratio of a shadow formed on the light receiving surface of one solar cell is plotted along the abscissa, and power (W) expended by one shadowed solar cell is plotted along the ordinate. Curves 29A, 29B and 29C correspond to a solar cell having parallel resistance of 20 kΩ/cm^2, 1 kΩ/cm^2 and 100 kΩ/cm^2, respectively. It is appreciated that the increase in temperature of a shadowed solar cell is greater as the power consumption is larger.

Fig. 30 is a graph showing the increase in temperature of one shadowed solar cell in a module having 36 solar cells connected in series. The ratio of a shadow to a light receiving surface is plotted along the abscissa, and the increase in temperature (°C) of a shadowed solar cell is plotted along the ordinate. Curve 30A shows the increase in temperature when the solar cell has a parallel resistance of 20 kΩ/cm^2. It is appreciated from curve 30A that the temperature of a shadowed solar cell is higher by 72°C than other solar cells when 20 % of the light receiving area is shadowed in the shadowed solar cell.

Fig. 30 relates to a solar cell module including 36 solar cells connected in series. The increase in temperature of a shadowed solar cell will further be increased in a solar cell module including a greater number of solar cells. In practice, there is sufficient possibility of 20 % of the light receiving area of one solar cell being shadowed.

Thus, it is understood that local shadowing in a solar cell module causes significant reduction in the output of the entire module. There is possibility of a shadowed solar cell being heated excessively to be damaged. In the worst case, a fire may break out. For example, in fine weather, the entire solar cell module rises to the temperature of 60°C to 70°C by solar heat. According to the example shown in Fig. 30, a solar cell having 20 % of the light receiving area shadowed may be heated up to 132°C to 142°C. In such a case, there is possibility of the EVA resin in which solar cells are imbedded being colored or pores being generated therein.

In order to prevent damage due to heating of such a shadowed solar cell, a solar cell module as shown in Fig. 31 is proposed. The solar cell module of Fig. 31(A) has rectangular solar cells 10 connected in series by interconnector 11. Fig. 31(B) is an enlarged perspective view of the portion indicated by the circle in (A). More specifically, adjacent solar cells 10 are connected by interconnector 11 via a bypass diode 15. Fig. 31(C) is an equivalent circuit diagram of solar cell 10 including bypass diode 15 of Fig. 31(B) (parallel resistance and serial resistance are not shown). It is appreciated from the circuit diagram that bypass diode 15 passes through current caused by reverse bias voltage applied to a shadowed solar cell 10. Therefore, excessive heating or short circuit breakdown can be prevented in a shadowed solar cell. However, the solar cell module of Fig. 31 has the disadvantage that the process of connecting the plurality of solar cells while attaching a bias diode is very complicated. Therefore, the manufacturing cost thereof is expensive.

The usage of solar cells having bypass diodes integrated (Japanese Patent Laying-Open No. 3-24768) and solar cells integrated so that zener diodes are connected in parallel with the same polarity (Japanese Patent Laying-Open No. 5-110121) are known for solar cell modules. However, such solar cells must have diodes formed therein using mask alignment, which is a complicated manufacturing process of the solar cell. This results in increase of the manufacturing cost.

SUMMARY OF THE INVENTION

In view of the foregoing, an object of the present invention is to provide a solar cell that can have significant reduction of the output of the entire module prevented when a solar cell is partially shadowed in a solar cell module.

Another object of the present invention is to provide a solar cell module improved to prevent excessive heating and short circuit breakdown caused by reverse bias voltage when a solar cell module is partially shadowed.

A further object of the present invention is to provide such an improved solar cell at a low cost using simple manufacturing steps.

A solar cell according to an aspect of the present invention includes: a p type semiconductor substrate having a first main surface, a second main surface, and a side face therebetween; a first n type layer formed on the first main surface; a p type layer formed on the second main surface and having an impurity concentration higher than that of the substrate; and a second n type layer formed at least on the side face so as to connect the first n type layer and the p type layer. The second n type layer has an impurity concentration lower than that of the first n type layer at least in the vicinity of the region in contact with the p type layer.

A method of manufacturing a solar cell according to another aspect of the present invention includes the steps of: preparing a p type semiconductor substrate having a first main surface, a second main surface, and a side face therebetween; applying an n type dopant agent on the first main surface; forming an n^+ type layer on the first main surface and an n type layer on the second main surface by applying a first thermal treatment to the substrate applied with a dopant agent; applying a paste layer including aluminum on the second main layer; and forming a p^+ type layer on the second main layer and an electrode by applying a second thermal treatment to the substrate having the paste layer including aluminum applied.

In the solar cell of the present invention, the connect region of the second n type layer and the p type layer form a small diode connected in parallel with a polarity identical to that of the solar cell formed of the p type substrate and the first n type layer. When the small diode is illuminated with light, a weak electromotive force of a polarity identical to that of the solar cell is generated. When a reverse bias voltage is applied to that solar cell, the small diode can pass through a current caused by the reverse bias voltage as leakage current since it has inferior reverse direction properties. More specifically, the solar cell of the present invention is characterized by including low parallel resistance when a reverse bias voltage is applied. Therefore, the usage of a solar cell of the present invention in a solar cell module prevents significant reduction in the output of the entire module even when the solar cell module is shadowed locally. Excessive heating and short circuit breakdown are avoided in a shadowed solar cell.

The manufacturing method of a solar cell according to the present invention does not require the resist printing step used for removing an n type layer formed on the back face and surface of a substrate of a conventional solar cell, an etching step, and a resist removal step. Therefore, a solar cell can be provided at low cost with a simple process.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a top view of a solar cell according to an embodiment of the present invention.

Fig. 2 is a back surface view of the solar cell of Fig. 1.

Fig. 3 shows sectional views of the manufacturing steps of the solar cell of Figs. 1 and 2.

Fig. 4 shows sectional views subsequent to the manufacturing step of Fig. 3.

Figs. 5 and 6 are elevation views showing examples of a spin coating method.

Fig. 7 is a sectional view of a plurality of silicon substrates arranged on a quartz board.

Fig. 8 is a graph showing the relationship between the maximum output and the sheet resistance of an n layer 2c of the solar cell shown in Fig. 2.

Fig. 9 shows sectional views of the manufacturing steps of a solar cell according to another embodiment of the present invention.

Fig. 10 shows sectional views of the manufacturing steps subsequent to Fig. 9.

Fig. 11 is an equivalent circuit diagram of a solar cell according to the present invention.

Fig. 12 is a graph showing the I-V characteristics of the solar cell of Fig. 11.

Fig. 13 is a graph showing the I-V characteristics actually measured of a solar cell obtained according to the present invention.

Fig. 14 is a graph showing the I-V characteristics of Fig. 13 divided into the I-V characteristics of the main components of the solar cell and the I-V characteristics of a parallel diode.

Fig. 15 is a graph showing the I-V characteristics in a solar cell module having 36 solar cells of the present invention connected in series.

Figs. 16 and 17 are graphs for describing the I-V characteristics in a solar cell module formed by solar cells having great parallel resistance and low parallel resistance, respectively.

Fig. 18 is a bottom view of a solar cell according to a further embodiment of the present invention.

Fig. 19 is a top view of a conventional solar cell.

Fig. 20 is a bottom view of the solar cell of Fig. 19.

Fig. 21 shows sectional views of the manufacturing step of the solar cell of Figs. 19 and 20.

Fig. 22 shows sectional views of the manufacturing process subsequent to Fig. 21.

Fig. 23 shows a solar cell module having 36 solar cells connected.

Fig. 24 is a graph showing the I-V characteristics in a solar cell having great parallel resistance.

Fig. 25 is an equivalent circuit diagram of a conventional solar cell.

Fig. 26 is a graph showing the I-V characteristics in a solar cell module formed by conventional solar cells.

Figs. 27 and 28 are graphs showing the power consumption of one shadowed solar cell in a solar cell module formed by solar cells having great parallel resistance and low parallel resistance, respectively.

Fig. 29 shows the relationship between power consumption and the ratio of the shadowed area in a shadowed solar cell module.

Fig. 30 is a graph showing the relationship between an increase in temperature and the shadowed area of one shadowed solar cell in a solar cell module.

Fig. 31 shows a conventional solar cell module including a bypass diode.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figs. 1 and 2 show a top view and a back surface view of a solar cell according to an embodiment of the present invention. The light receiving surface of a solar cell 10A of Fig. 1 has a structure identical to that of solar cell 10 of Fig. 19. Solar cell 10A of Fig. 2 differs from solar cell 10 of Fig. 20 in that an n type semiconductor layer 2C is formed at the peripheral edge portion of the back surface.

Figs. 3 and 4 show the manufacturing steps of the solar cell shown in Figs. 1 and 2. The step of Fig. 3(A) is identical to that shown in Fig. 21(A), so that their description will not be repeated.

Referring to Fig. 3(B), a dopant agent layer 20 is applied on the top face of a semiconductor substrate 1 by a spin coater. A solution including, for example, 80 mℓ of tetra isopropyl titanate, 2000 mℓ of isopropyl alcohol, and 45 g of phosphorus pentaoxide may be used as this dopant agent. The amount of phosphorus pentaoxide is selected within the range of 20 g to 70 g depending upon the diffusion condition in order to form an n layer of a desired impurity concentration (normally, 10^{19} to 10^{20} cm^{-3}) at the top face of substrate 1.

Such a dopant agent 20 can be applied on semiconductor substrate 1 by a spin coating method shown in Fig. 5. Semiconductor substrate 1 is attracted via a tube along the rotary shaft of a spin chuck 21. Substrate 1 held by spin chuck 21 is rotated at approximately 5000 rpm, and dopant solution 20 is applied dropwise onto substrate 1 via a nozzle 22. Dopant solution 20 dropped on substrate 1 spreads all over the top surface of semiconductor substrate 1 by the centrifugal force.

A plurality of the semiconductor substrates of Fig. 3(B) having dopant agent 20 applied are set on a quartz board 30 shown in Fig. 7. Here, the plurality of semiconductor substrates 1 are set so that the main surface on which the dopant agent is applied faces the same direction. The distance between each substrate 1 is adjusted to be within the range of 2.0 mm to 5.0 mm. Quartz board 30 is inserted into a quartz tube 31. In quartz tube 31, N_2 gas including 0.5 % to 10 % of O_2 gas is provided. Preferably, the concentration range of O_2 gas is 1 % to 5 %. Under this condition, the plurality of semiconductor substrates 1 are subjected to a thermal treatment for 45 minutes at 900 °C, for example.

Fig. 3(C) shows the results of the thermal treatment shown in Fig. 7. On the top surface of semiconductor substrate 1, an n^+ layer 2a of a thickness of approximately 0.4 µm and an anti-reflection film 3 of TiO_2 having a thickness of approximately 70 - 80 nm are formed simultaneously. Here, n type layers 2b and 2c are formed at the side face and the bottom surface, respectively, of substrate 1 due to automatic doping according to out-diffusion from dopant agent 20. n layers 2b and 2c formed by automatic doping have an impurity concentration lower than that of n^+ layer 2a formed by direct diffusion from dopant agent 20. Furthermore, a thin oxide film 1a of 20 Å - 100 Å (the thickness of this oxide film is not shown in the drawing) is formed at the surfaces of n layers 2b and 2c. This oxide film can be used as a passivation film.

Referring to Fig. 4(A), paste 5 including silver and paste 6 including aluminum are printed at a predetermined pattern on the back surface of substrate 1. The peripheral edge of paste layer 6 including aluminum retreats by 1 mm - 4 mm from the peripheral edge of substrate 1. After the printed paste is dried, a baking process at the temperature of 700 °C - 750 °C is carried out, whereby a back

aluminum electrode 6 of approximately 50 μm in thickness and a back silver electrode 5 of approximately 20 μm in thickness are formed. Here, a p^+ layer 7 of approximately 5 μm in thickness is formed on aluminum electrode 6. This p^+ layer 7 serves to generate the BSF effect of a solar cell.

Referring to Fig. 4(B), paste 8 including silver is printed with a pattern identical to that of pattern 8a of Fig. 1. The peripheral edge of paste pattern 8 retreats by 1 mm - 3 mm from the peripheral edge of substrate 1. Paste pattern 8 is baked at a temperature of 650°C - 750°C, whereby a front silver electrode 8 is formed. Here, the paste including silver also includes glass frit, so that silver electrode 8 forms an ohmic contact with n^+ layer 2a through anti-reflection film 3.

Referring to Fig. 4(C), semiconductor substrate 1 is dipped in a solder tank of approximately 190°C, whereby silver electrodes 5 and 8 are covered with solder layers 5a and 8a, respectively, of approximately 20 μm in thickness. Thus, the solar cell shown in Figs. 1 and 2 is completed. The sectional view of Fig. 4(C) corresponds to the structure of Fig. 2 taken along line 4F - 4F.

Fig. 8 is a graph showing the relationship between the maximum output and the sheet resistance of the back face n layer 2c in the solar cell of Fig. 4(C). The maximum output (W) of the solar cell is plotted along the abscissa, and the sheet resistance (Ω/□) of n layer 2c on the back surface is plotted along the ordinate. It is appreciated from Fig. 8 that the solar cell exhibits high and stable maximum output when the sheet resistance of n layer 2c becomes greater than 70 Ω/□. However, if the sheet resistance of n layer 2c is too great, the solar cell will have great parallel resistance, so that the object of the present invention cannot be achieved. Therefore, the sheet resistance of n layer 2c is preferably within the range of 70 - 300 Ω/□. More preferably, the sheet resistance of n layer 2c is within the range of 70 - 200 Ω/□ in order to further facilitate the current flow when a reverse bias voltage is applied to the solar cell.

The sheet resistance of n layer 2c at the back surface of substrate 1 can be controlled by adjusting the diffusion conditions such as the oxygen partial pressure and the distance between the substrates during the diffusion step shown in Figs. 3(C) and 7.

In contrast to the manufacturing steps shown in Figs. 21 and 22, it is appreciated that the embodiment shown in Figs. 3 and 4 do not require the respective anti-reflection film formation steps shown in Fig. 21(C) since anti-reflection film 3 is formed at the same time n type layers 2a, 2b and 2c are formed as shown in Fig. 3(C), and also the resist printing step and etching step shown in Fig. 21(D), and the resist removal step shown in Fig. 22(E). More specifically, the manufacturing steps of the embodiment shown in Figs. 3 and 4 are extremely simplified in comparison with the steps by prior art shown in Figs. 23 and 24. Therefore, a solar cell can be manufactured at low cost.

Figs. 9 and 10 show manufacturing step of a solar cell according to another embodiment of the present invention.

Referring to Fig. 9(A), a p type silicon substrate 1 similar to that of Fig. 3(A) is prepared.

Referring to Fig. 9(B), a dopant agent layer 20 is applied on the top face of substrate 1, and an incomplete mask layer is applied at the peripheral edge portion of the bottom surface. Dopant agent 20 can be applied, as shown in Fig. 6, using a spin coater as in the step of Fig. 3(B). It is to be noted that in Fig. 9(B), a mask material 23 is applied from nozzle 24 to the peripheral edge portion of the back surface of substrate 1.

A solution including 100 mℓ of ethyl silicate, 50 mℓ of acetic acid, and 500 mℓ of ethyl alcohol, for example, can be used as mask material 23. Mask material 23 may include 1 g - 10 g of phosphorus pentaoxide in order to prevent mask layer 23 from functioning as a complete mask and to ensure slight diffusion of n type dopants. Mask material 23 may include alkyl titanate instead of alkyl silicate such as ethyl silicate.

Referring to Fig. 9(C), substrate 1 having dopant agent layer 20 and mask layer 23 applied is subjected to a thermal treatment for 45 minutes at 900°C, for example. As a result, n type layer 2a of a high impurity concentration and anti-reflection film 3 are formed on substrate 1. n type layers 2b and 2c having an impurity concentration lower than that of n type layer 2a are formed at the side face and the bottom surface, respectively, of substrate 1. An n type layer 2d having a thickness and impurity concentration smaller than those of the bottom face n type layer 2c is formed beneath mask layer 23.

The manufacturing steps shown in (A) to (C) of Fig. 10 are similar to those of Fig. 4, and their description will not be repeated.

The manufacturing method of a solar cell shown in Figs. 9 and 10 can be applied to a vapor diffusion method using $POCℓ_3$ gas. In this case, the application of dopant agent layer 20 on substrate 1 is omitted, and vapor diffusion is carried out using $POCℓ_3$ gas after mask layer 23 is provided.

Although the embodiment of Figs. 9 and 10 was described in which mask layer 23 is not removed, mask layer 23 may be removed using a weak hydrofluoric acid. Mask solution 23 can be obtained by mixing a main solution described below and a solution including titanium or silicon. An additional solution may further be mixed if desired.

As the main solution, an alcohol group such as isopropyl alcohol, ethyl alcohol, methyl alcohol, and butyl alcohol or a ketone group such as methyl ethyl ketone can be used.

As a solution including titanium, tetra isopropyl titanate, tetra n-butyl titanate, titanium chloride, etc. can be used. Furthermore, a solution having powder such as titanium, titanium boride, titanium carbide, and titanium dioxide mixed into acid, alkali, alcohol, ester, etc. can be used.

Ethyl silicate, methyl silicate, and isopropyl silicate can be used for the solution including silicon. Furthermore, a solution including a halide of silicon can be used.

As the additional solution, carboxylic acid such as formic acid, acetic acid, oxalic acid, benzoic acid, etc. can be used.

As dopant agent 20, a mixture of the above-described main solution and a solution including titanium added with an appropriate amount of phosphorus source such as phosphorus pentaoxide or oxy phosphorus chloride can be used. For example, phosphorus of 1.04 - 3.63 gram atoms are added per 1 mol of TiO_2 in a solution including titanium, and the alcohol group as the main solution has the mixed rate determined according to the number of revolution of the spin coater to obtain the dopant agent layer 20 of a desired thickness (for example 70 - 80 nm). A more preferable mixed rate of phosphorus is 2.2 - 2.5 gram atom per 1 mol of TiO_2. This value is selected since front silver electrode 8 cannot easily pierce anti-reflection film 3 if the phosphorus concentration is too low, and control of the impurity concentration of the n layer formed at the side face and the back surface of the substrate will become difficult due to significant out-diffusion if the phosphorus concentration is too high. More specifically, a preferable example of a dopant solution is a mixture of 80 mℓ tetra isopropyl titanate (corresponding to 28 % TiO_2), 2000 mℓ of isopropyl alcohol, and 45 g of phosphorus pentaoxide.

Fig. 11 shows an equivalent circuit diagram of a solar cell according to the present invention. Solar cell 11A includes a diode 11B in parallel in addition to parallel resistance and serial resistance. Solar cell 11A is formed of a p type substrate 1 and an n^+ layer 2a. Parallel diode 11B is formed of a p^+ layer 7 and an n layer 2c in the embodiment of Fig. 4(C), and a p^+ layer 7 and an n layer 2d in the embodiment of Fig. 10(C). In such a solar cell, parallel diode 11B serves as a solar cell when illuminated with light. However, when the solar cell is shadowed and a reverse bias voltage is applied across nodes 11C and 11D, a relatively large leakage current can be conducted from node 11D to node 11C since parallel diode 11B has inferior reverse direction properties. More specifically, the solar cell shown in Fig. 11 is equivalent to including extremely low parallel resistance when shadowed.

Fig. 12 shows the I-V characteristics in a qualitative manner of the solar cell of Fig. 11. Curve 12A and 12B show the I-V characteristics of a solar cell when not shadowed and when completely shadowed, respectively. By comparing curve 12B with curve 24B of Fig. 24, it is appreciated that the solar cell of Fig. 11 can conduct a greater current flow when a reverse bias voltage is applied in comparison with the solar cell of Fig. 25.

Fig. 13 shows an example of the I-V characteristics measured by a solar cell obtained according to the present invention. It is appreciated that the solar cell of the present invention having an extremely low parallel resistance has photoelectric conversion efficiency identical to that of a solar cell having a great high parallel resistance.

Fig. 14 is a graph showing two I-V characteristics obtained by dividing the curve shown in Fig. 13. More specifically, curve 14A shows the I-V characteristics of solar cell 11A of Fig. 11, and curve 14B shows the I-V characteristics of parallel diode 11B. It can be considered that the I-V characteristics of Fig. 13 are obtained as a result of combining the I-V characteristics of solar cell 11A of Fig. 11 and the I-V characteristics of parallel diode 11B.

Fig. 15 shows the I-V characteristics when one solar cell is shadowed in a solar cell module including 36 solar cells of the present invention. The present solar cell has a parallel resistance of approximately 100 Ω/cm^2 including the parallel diode. The value of the % shown in the graph represents the ratio of a shadowed area with respect to the light receiving surface of one solar cell. It is appreciated from the graph of Fig. 15 that the output of the solar cell module is reduced by just approximately 30 % even when one solar cell is completely shadowed. By comparing Figs. 15 and 26, it is appreciated that a solar cell module using the solar cells of the present invention has reduction of an output extremely suppressed when shadowed in comparison with that of a conventional solar cell module.

This can be understood more easily by comparing Figs. 16 and 17. Fig. 16 shows the I-V characteristics in a solar cell module using solar cells having high parallel resistance. In (A), curve 16B shows the I-V characteristics of one solar cell completely shadowed. Curve 16A shows the I-V characteristics of n solar cells connected in series. V_A represents the voltage of curve 16A, and V_B represents the voltage of curve 168. In (B), curve 16C shows the I-V characteristics which is a combination of curves 16A and 16B. It can be appreciated that the output current of (n + 1) solar cells connected in series is significantly reduced since

the shadowed solar cell has a great parallel resistance.

Fig. 17 shows the I-V characteristics in a solar cell module using the solar cells of the present invention. In Fig. 17(A), curve 17A is similar to curve 16 in Fig. 16(A), showing the I-V characteristics of n solar cells connected in series. In contrast, curve 17B shows the I-V characteristics when one solar cell having an extremely low small parallel resistance (100 Ω/cm^2) is completely shadowed. More specifically, since this solar cell has a low parallel resistance, a current according to a reverse bias voltage, when applied, can be easily conducted. In Fig. 17(B), curve 17C shows the I-V characteristics of a solar cell module including (n + 1) solar cells connected in series obtained by combining curves 17A and 17B. By comparing Figs. 17(B) and 16(B), reduction in the output of the entire solar cell module is significantly suppressed even if one solar cell is shadowed when the solar cell has a low parallel resistance.

Line 30B in Fig. 30 shows the relationship between the shadowed area of one solar cell and an increase in temperature within a solar cell module having 36 solar cells of the present invention connected. It is appreciated that, even when one solar cell is completely shadowed in a solar cell module including 36 solar cells of the present invention, increase in temperature of that solar cell is only 11 °C in comparison with the other solar cells. This is because current due to reverse bias voltage flows easily since the parallel resistance of the shadowed solar cell is low.

When the parallel resistance is to be further reduced in a solar cell of the present invention shown in Fig. 2, the peripheral edge of aluminum electrode pattern 6 can be formed in a waveform manner as shown in Fig. 18 to increase the contact interface between n layer 2C and p^+ layer 7 shown in Fig. 4(C).

Paste 6 including aluminum may include silver paste including several % of aluminum.

According to the present invention, a solar cell can be provided that has a photoelectric conversion efficiency equal to that of a conventional solar cell, and that can have the adverse effect of a shadow reduced significantly when used in a solar cell module. More specifically, in a solar cell module using a solar cell of the present invention, reduction of output when locally shadowed can be suppressed significantly. Also, excessive heating of a shadowed solar cell in a solar cell module can be prevented. Therefore, the disadvantage of short circuit breakdown of the solar cell and the possibility of fire can be avoided.

According to the present invention, a solar cell that can exhibit superior effects when used in a solar cell module can be provided with a simple process at low cost.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

Claims

1. A solar cell comprising:

   p type semiconductor substrate (1) including a first main surface, a second main surface, and a side face therebetween,

   a first n type layer (2a) formed on said first main surface,

   a p type layer (7) formed on said second main surface and having an impurity concentration higher than that of said substrate (1), and

   a second n type layer (2b, 2c, 2d) formed at least on said side face so as to connect said first n type layer (2a) with said p type layer (7), wherein said second n type layer (2b, 2c, 2d) has an impurity concentration lower than that of said first n type layer (2a) at least in the proximity of a region in contact with said p type layer (7).

2. The solar cell according to claim 1, wherein said second n type layer (2b, 2c, 2d) has a sheet resistance within the range of 70 to 300 $\Omega/\square$ at least in the proximity of a region in contact with said p type layer (7).

3. The solar cell according to claim 1 or 2, wherein said second n type layer (2b, 2c, 2d) extends to a peripheral edge of said second main surface as well as on said side face.

4. The solar cell according to any of claims 1 to 3, wherein said second n type layer (2b, 2c, 2d) and said p type layer (7) are connected on said second main surface, the connecting surface thereof being formed in a waveform manner in order to increase the connecting area.

5. A method of manufacturing a solar cell comprising the steps of:

   preparing a p type semiconductor substrate (1) including a first main surface, a second main surface, and a side face therebetween,

   applying an n type dopant agent (20) on said first main surface,

   forming an n^+ type layer (2a) on said first main surface and an n type layer (2b, 2c, 2d)

on said side face and said second main surface by applying a first thermal treatment to said substrate (1) applied with said dopant agent (20),

applying a paste layer including aluminum on said second main surface,

forming a p^+ type layer (7) on said second main surface and forming an electrode (6) by applying a second thermal treatment to said substrate (1) applied with said paste layer including aluminum.

6. The manufacturing method of a solar cell according to claim 5, wherein an incomplete mask layer (23) is applied at a peripheral edge of said second main surface in applying said n type dopant agent (20) on said first main layer, wherein said second n type layer (2b, 2c, 2d) formed by said first thermal treatment has the thickness and impurity concentration reduced in a region (2d) below said mask layer (23).

7. The manufacturing method of a solar cell according to claim 5 or 6, wherein said dopant agent (20) comprises a solution including phosphorus in the range of 1.04 - 0.63 gram atoms per 1 mol of TiO_2, and wherein said n^+ type layer (2a) on said first main surface and an anti-reflection (3) film of TiO_2 are formed at said first thermal treatment.

8. The manufacturing method of a solar cell according to any of claims 5 to 7, wherein oxygen of a predetermined partial pressure is introduced during said first thermal treatment, and an oxide passivation film is formed at the surface of said substrate.

FIG. 1

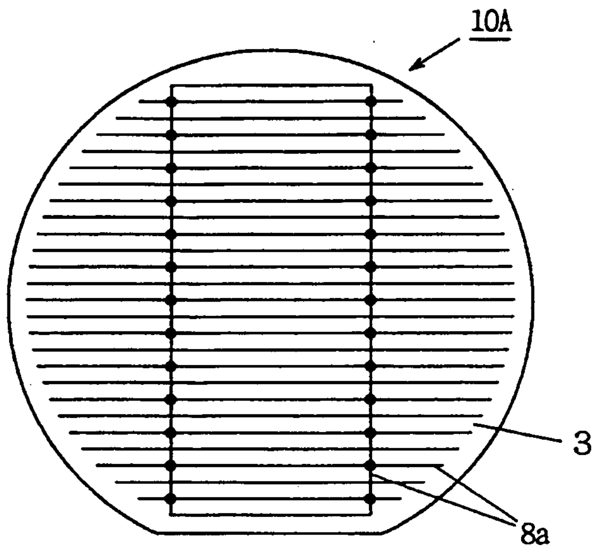


FIG. 2

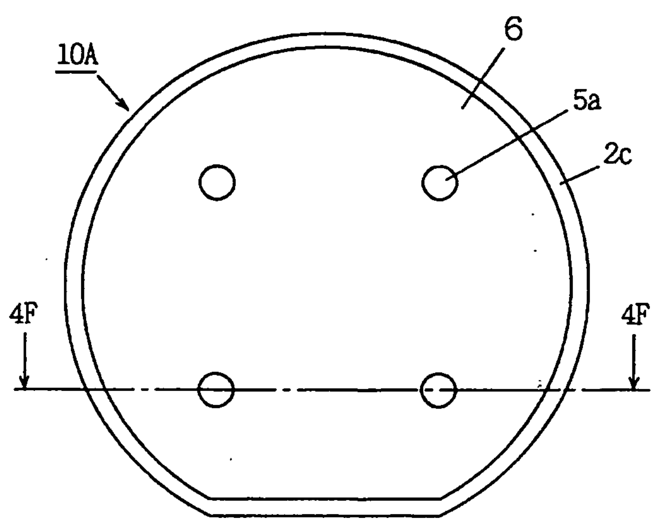


FIG. 3

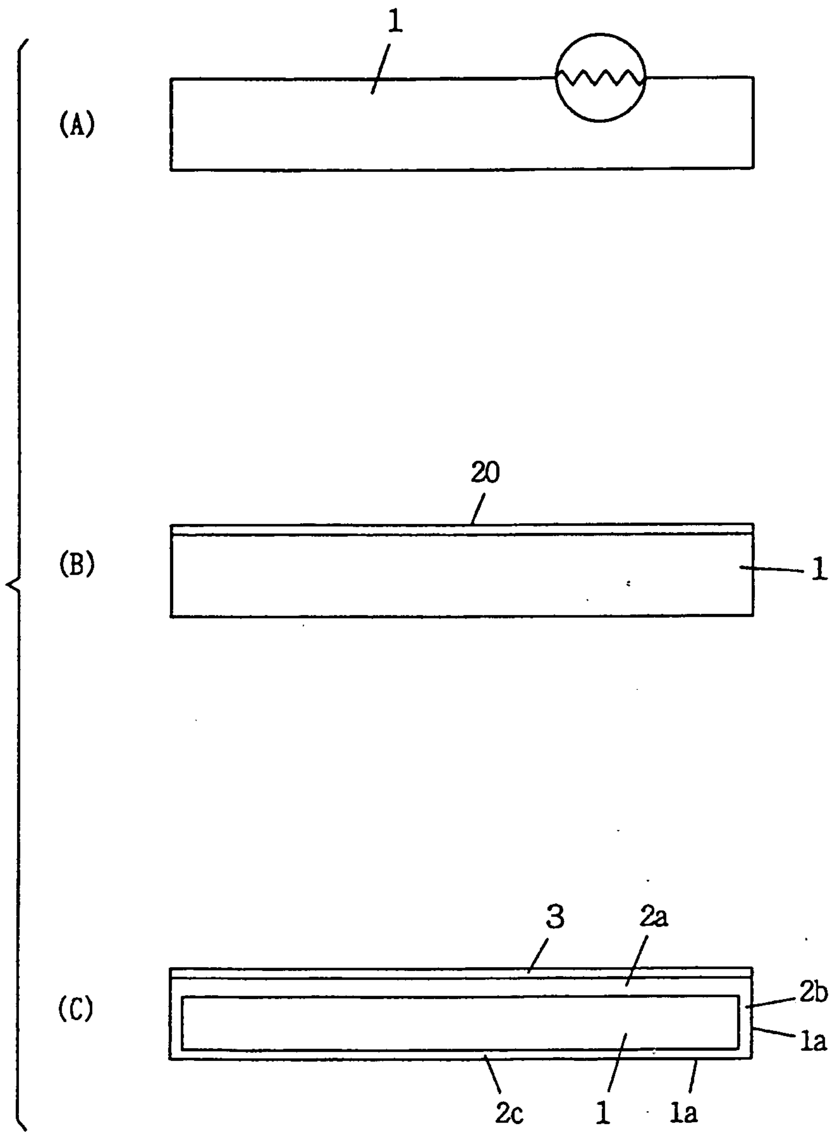


FIG. 4

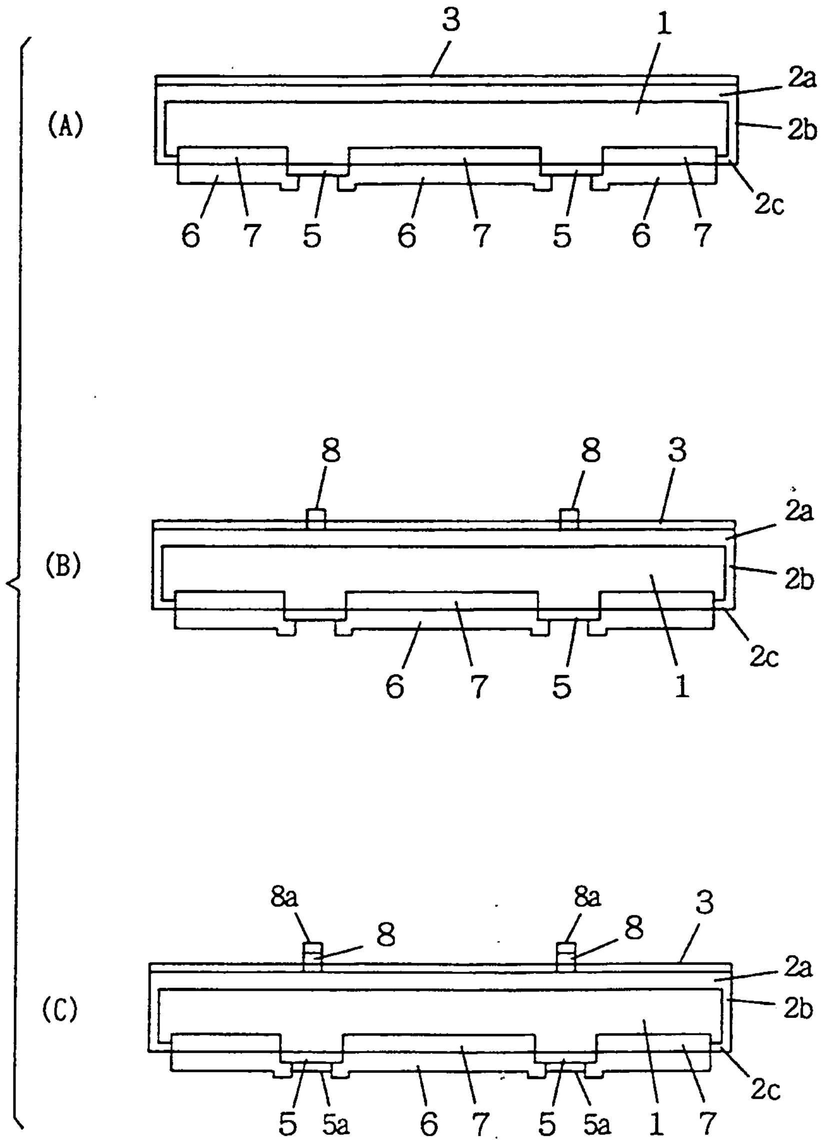

(A)
3
1
2a
2b
2c
6
7
5
6
7
5
6
7
(B)
8
8
3
2a
2b
2c
6
7
5
1
(C)
8a
8
8a
8
3
2a
2b
2c
5
5a
6
7
5
5a
1
7

FIG. 5

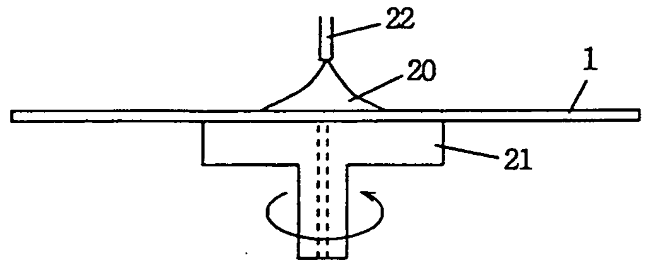


FIG. 6

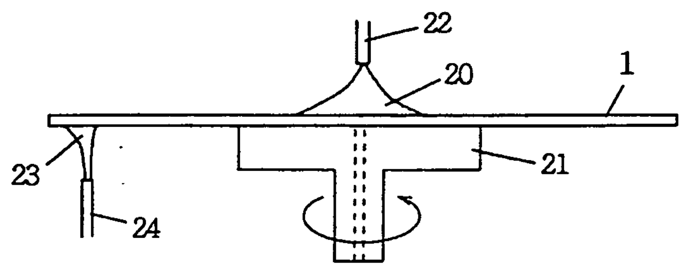


FIG. 7

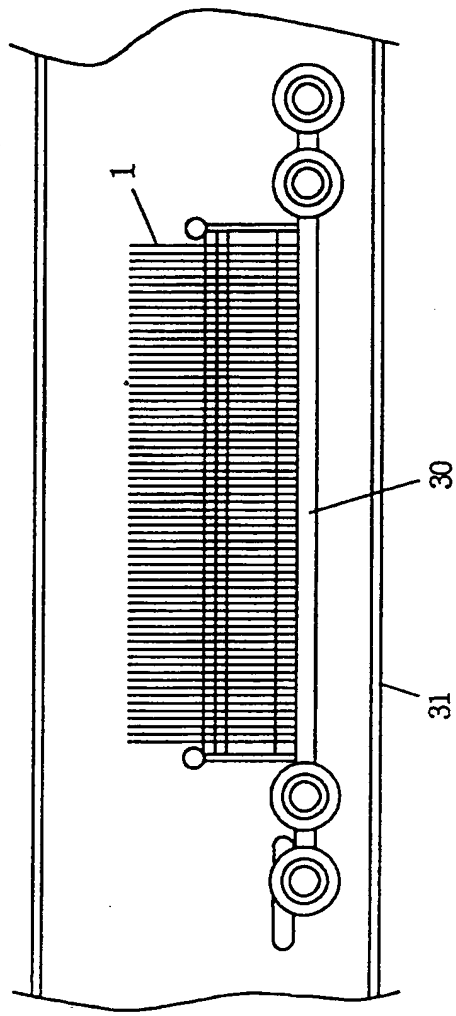


FIG. 8

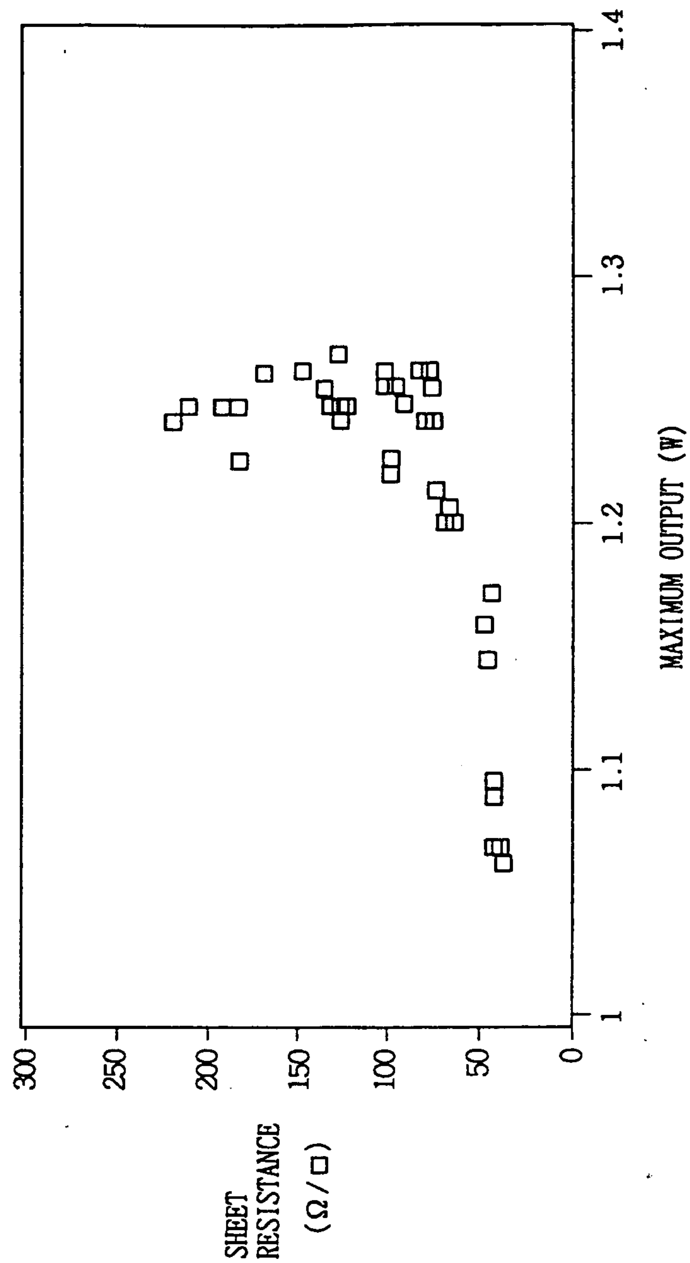

300
250
200
150
100
50
0
1
1.1
1.2
1.3
1.4
MAXIMUM OUTPUT (W)
SHEET RESISTANCE (Ω/□)

FIG. 9

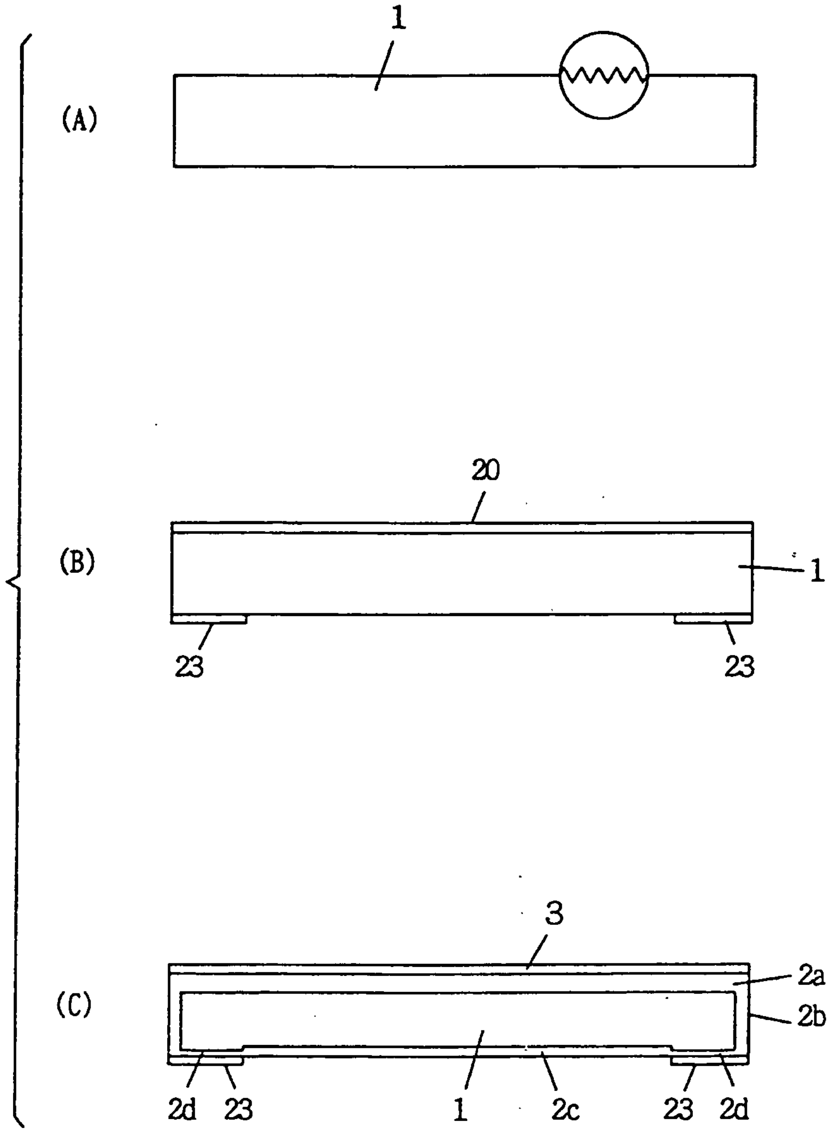


FIG. 10

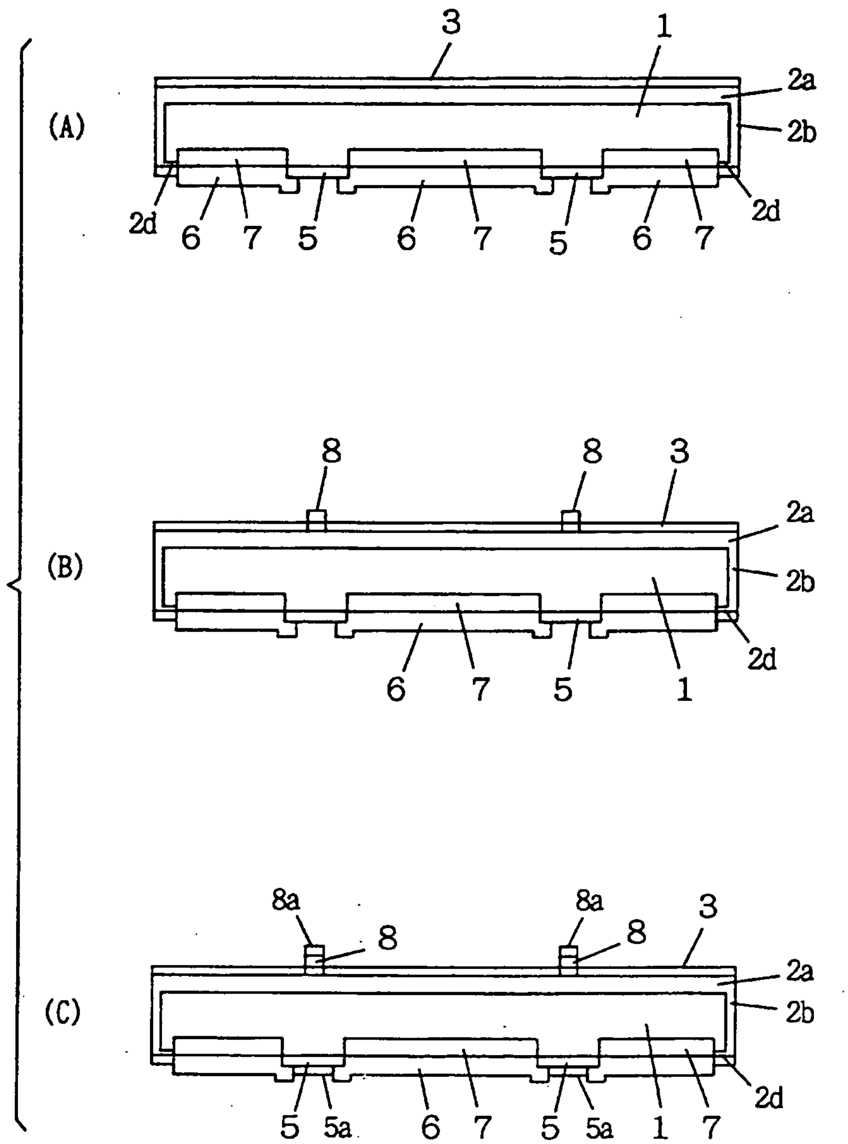

(A)
3
1
2a
2b
2d
6
7
5
6
7
5
6
7
2d
(B)
8
8
3
2a
2b
6
7
5
1
2d
(C)
8a
8
8a
8
3
2a
2b
5
5a
6
7
5
5a
1
7
2d

FIG. 11

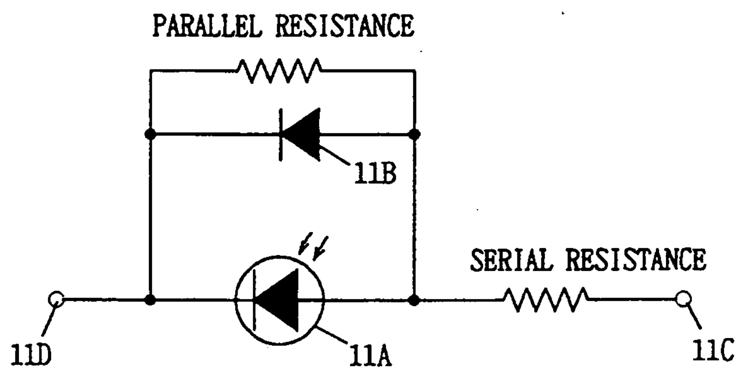

PARALLEL RESISTANCE
11B
SERIAL RESISTANCE
11D
11A
11C

FIG. 12

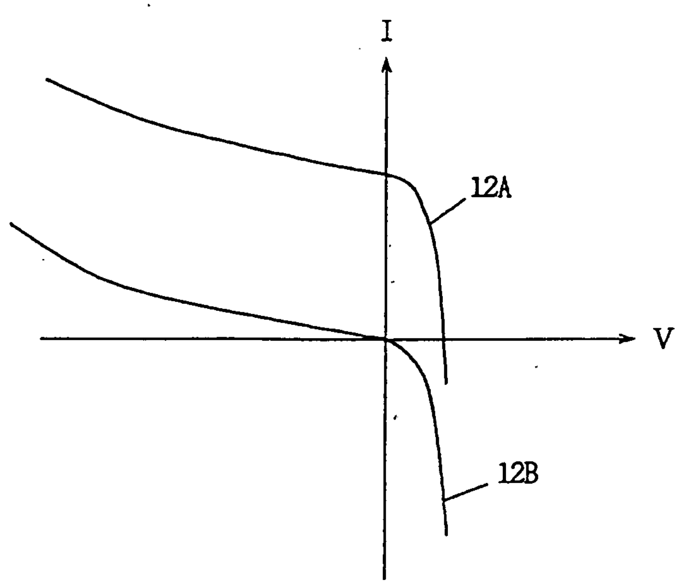

I
12A
V
12B

FIG. 13

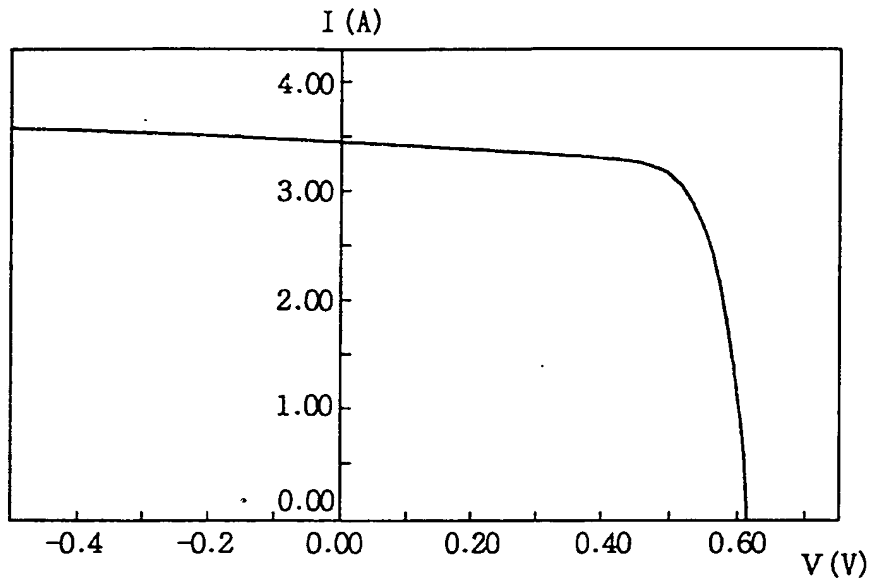

I (A)
4.00
3.00
2.00
1.00
0.00
-0.4
-0.2
0.00
0.20
0.40
0.60
V (V)

FIG. 14

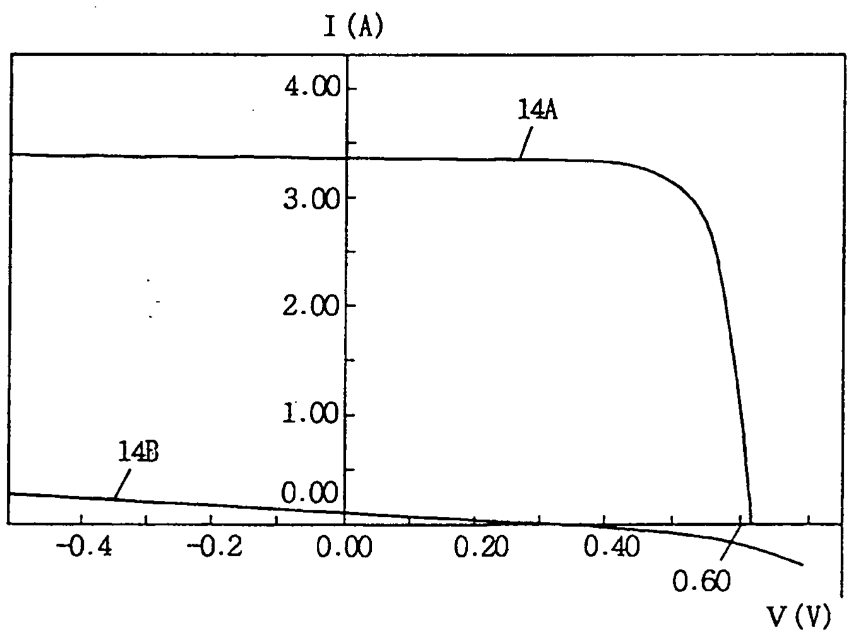

I (A)
4.00
3.00
2.00
1.00
0.00
14A
14B
-0.4
-0.2
0.00
0.20
0.40
0.60
V (V)

FIG. 15

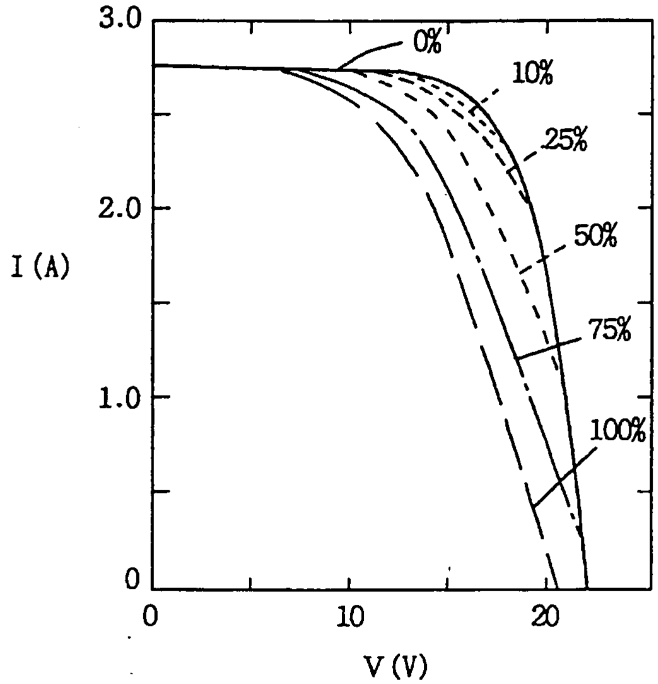


FIG. 16

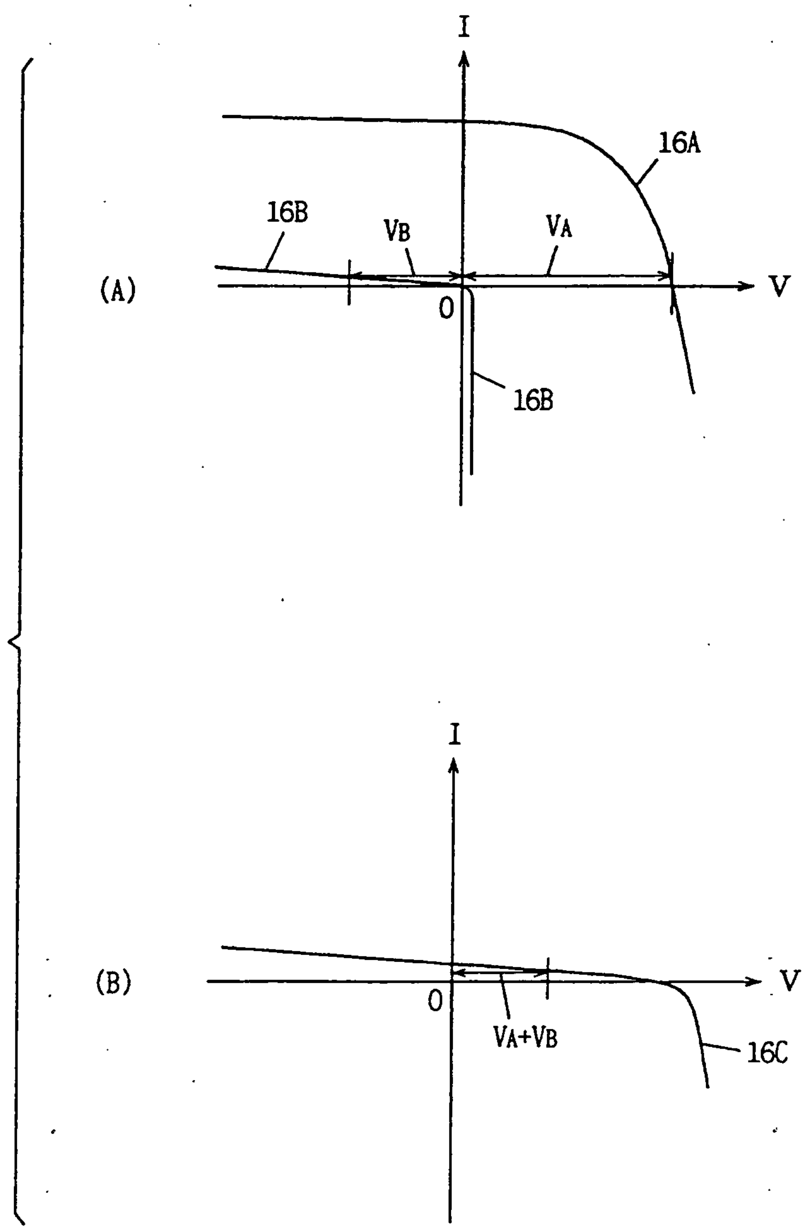


FIG. 17

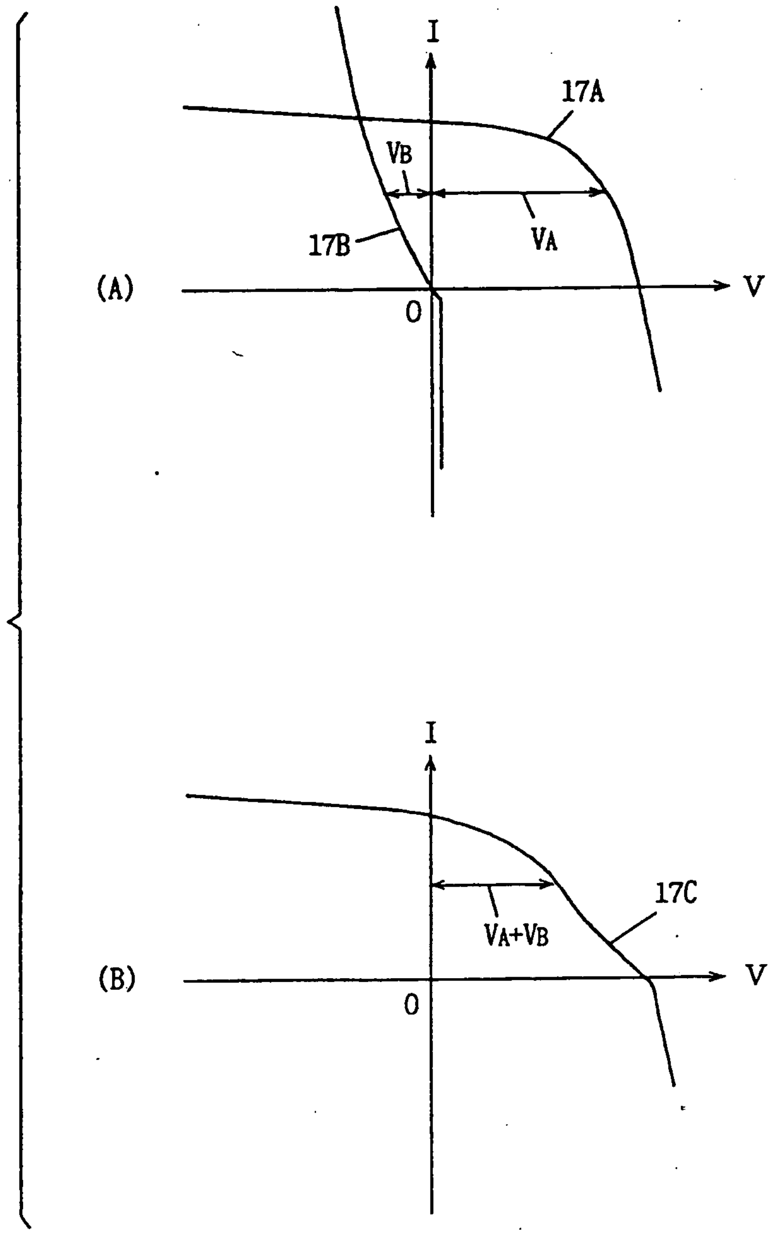


FIG. 18

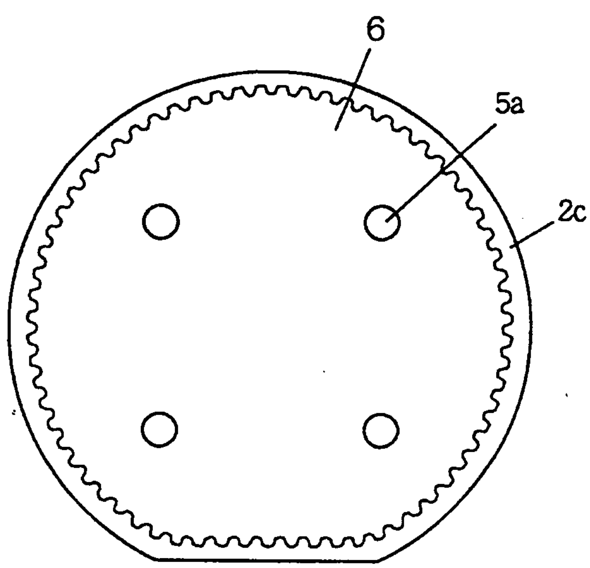


FIG. 19

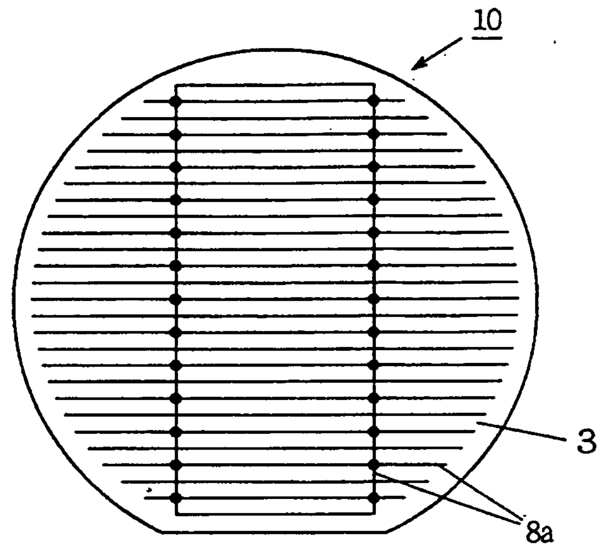


FIG. 20

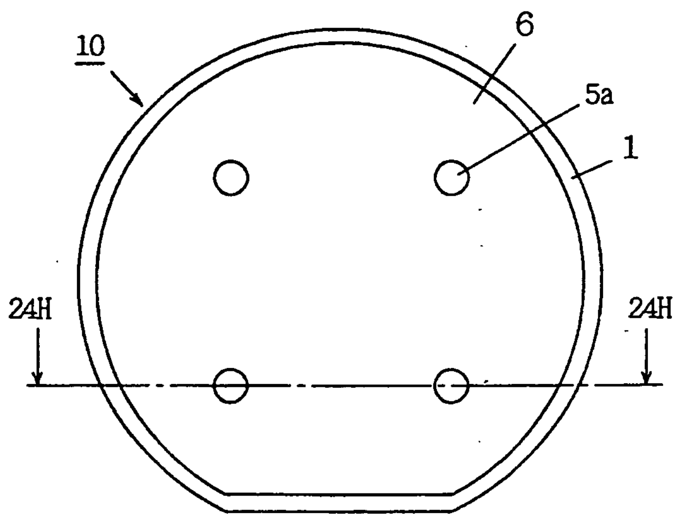


FIG. 21

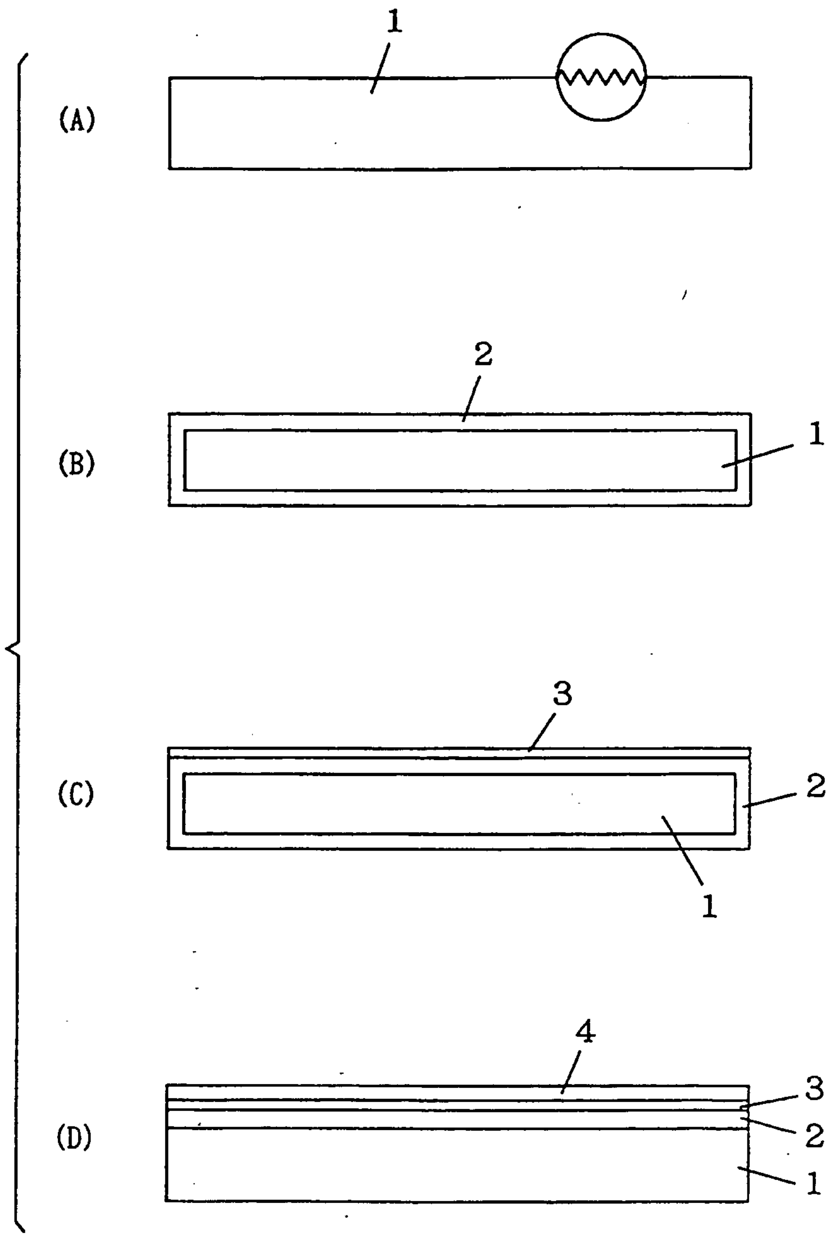


FIG. 22

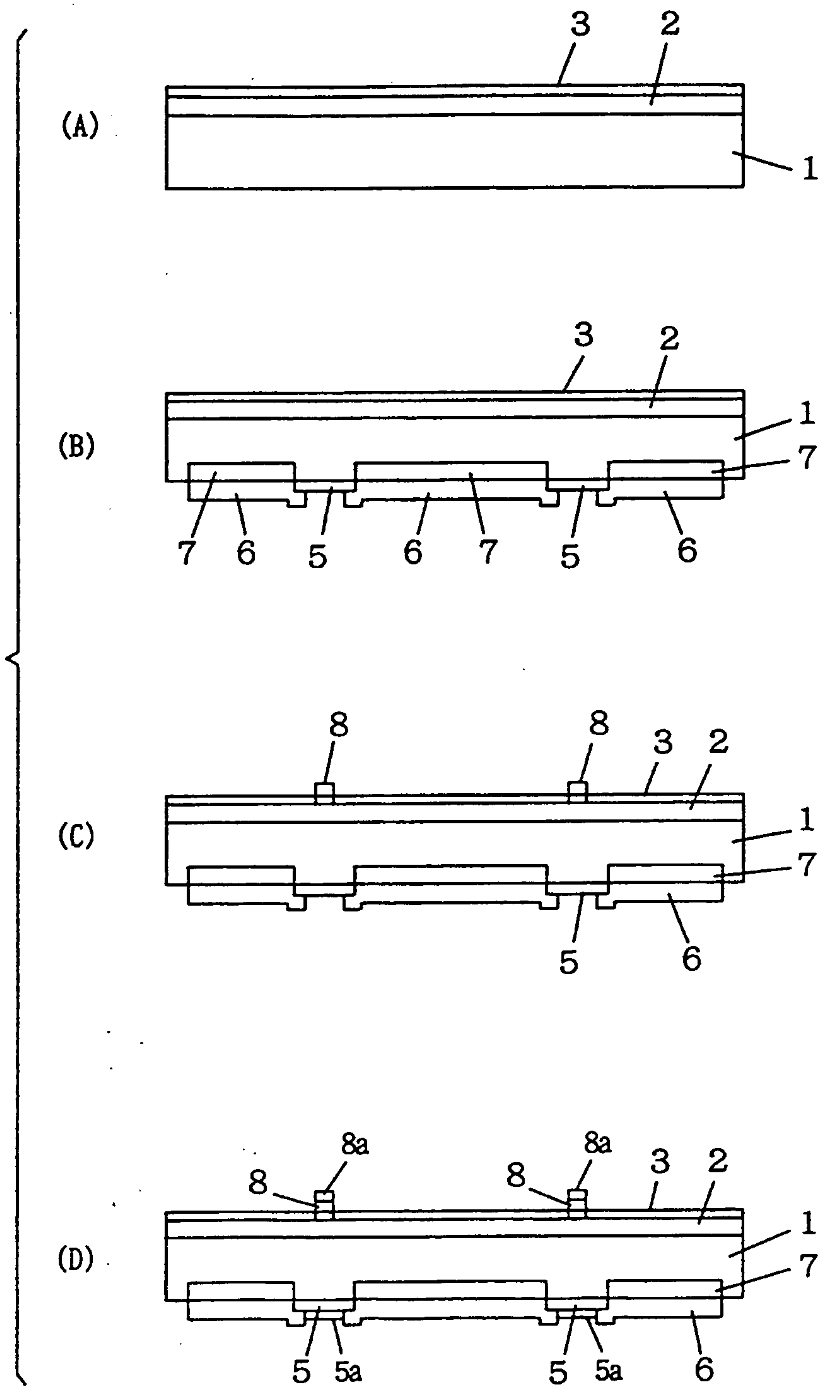


FIG. 23

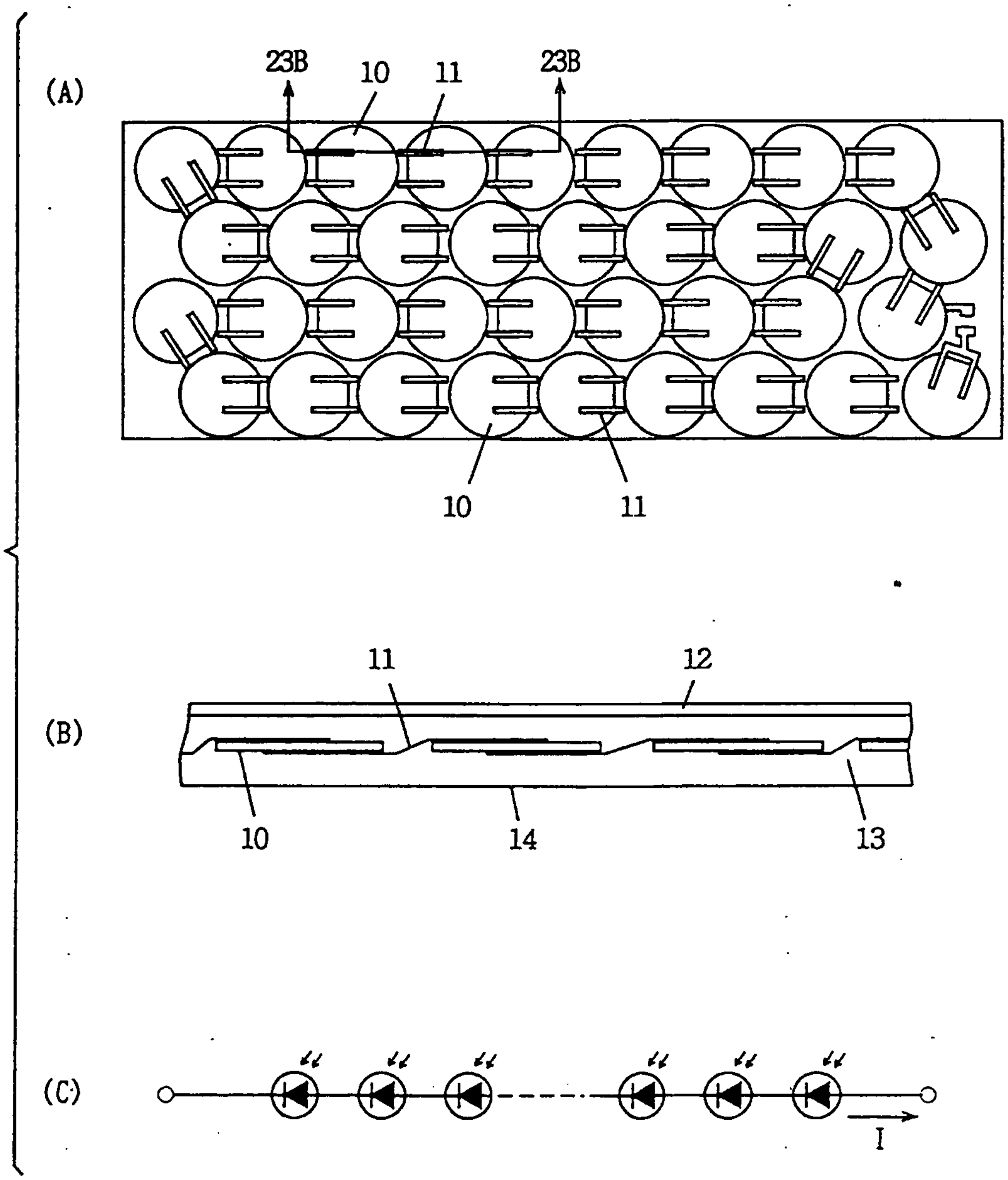


FIG. 24

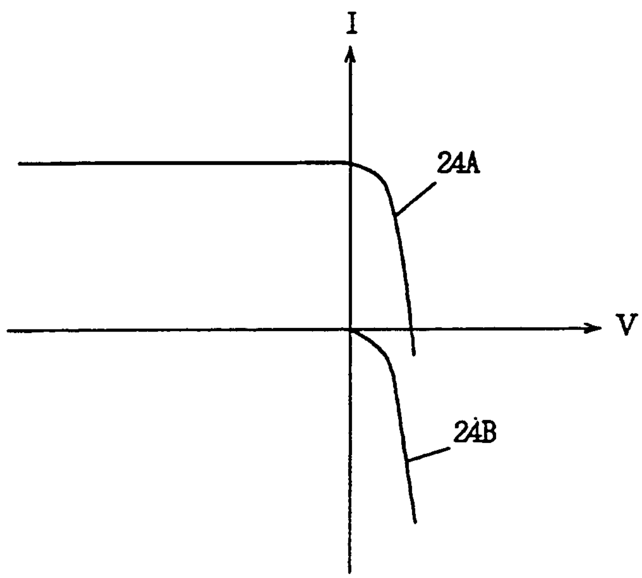


FIG. 25

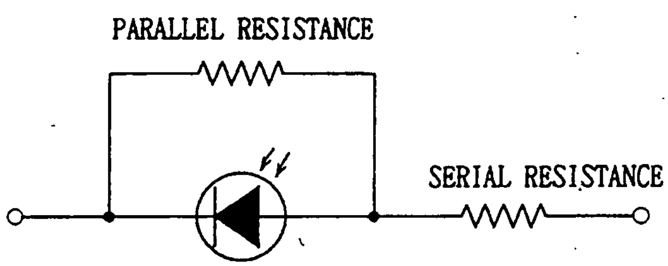


FIG. 26

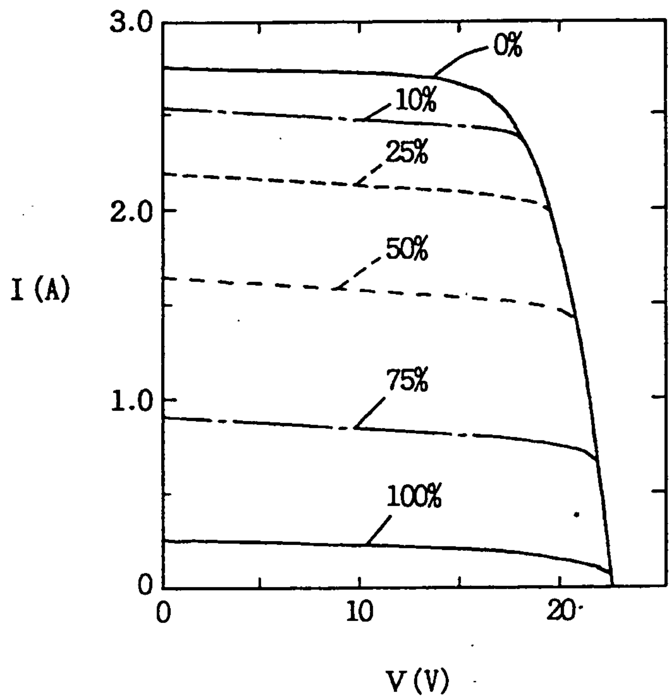


FIG. 27

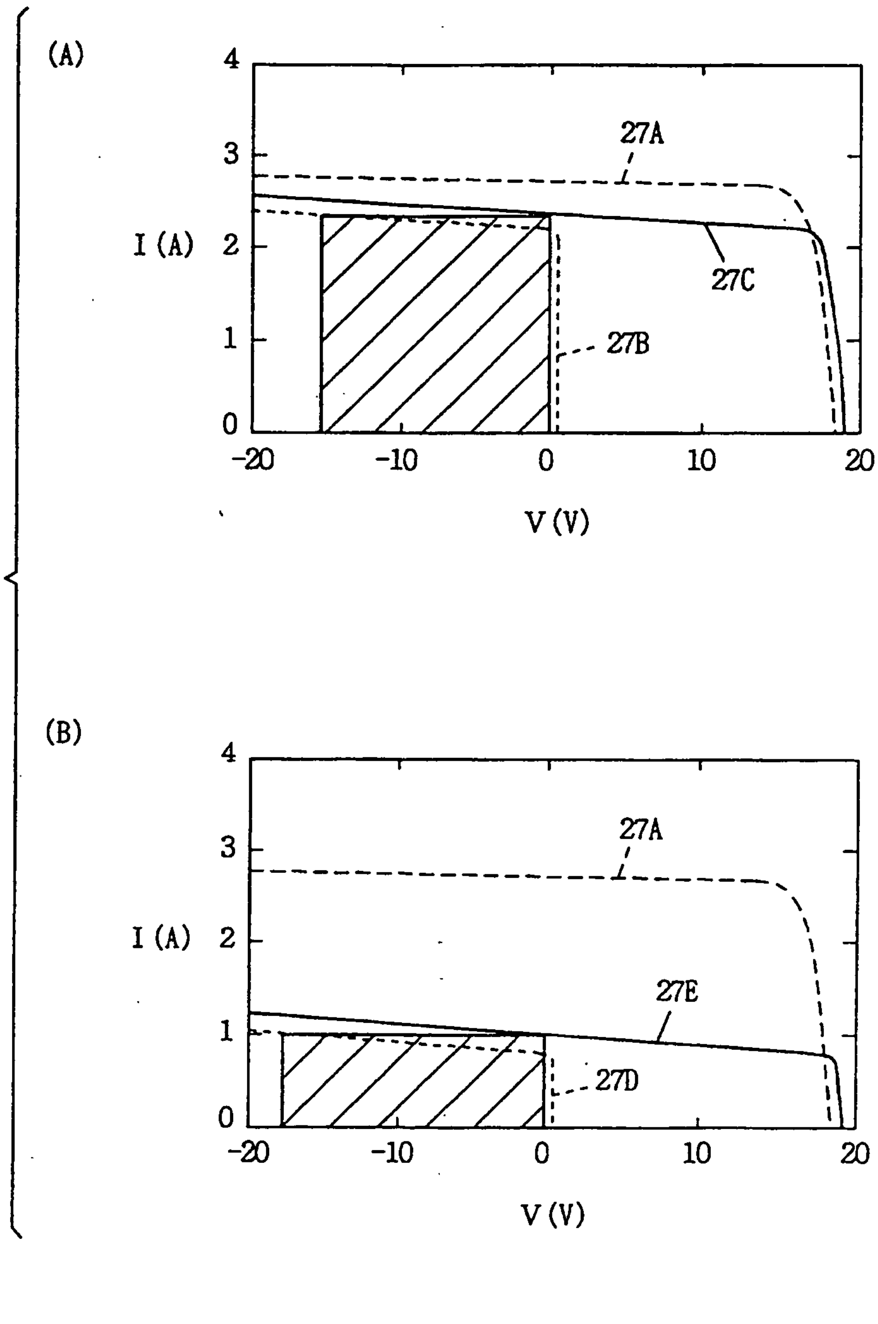

(A)
4
3
2
1
0
I (A)
-20
-10
0
10
20
V (V)
27A
27B
27C
(B)
4
3
2
1
0
I (A)
-20
-10
0
10
20
V (V)
27A
27D
27E

FIG. 28

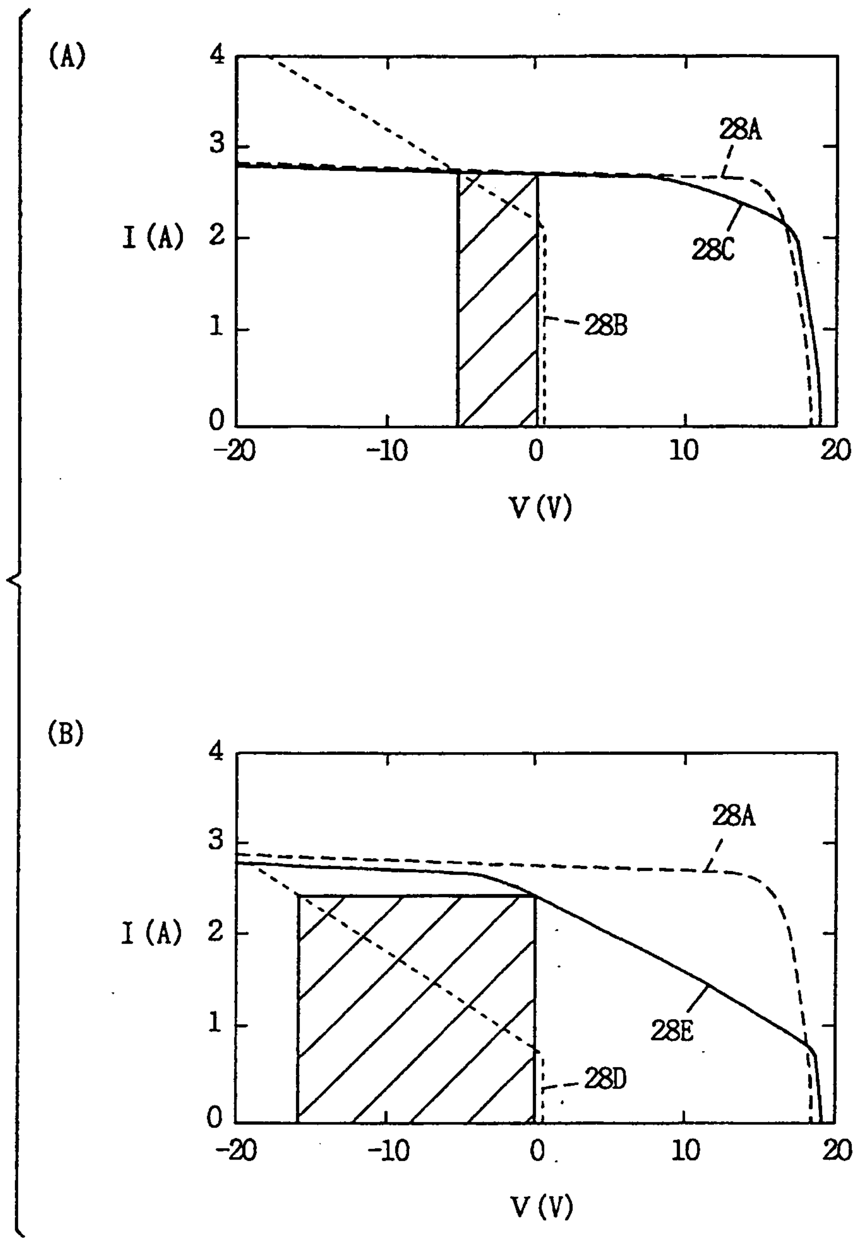
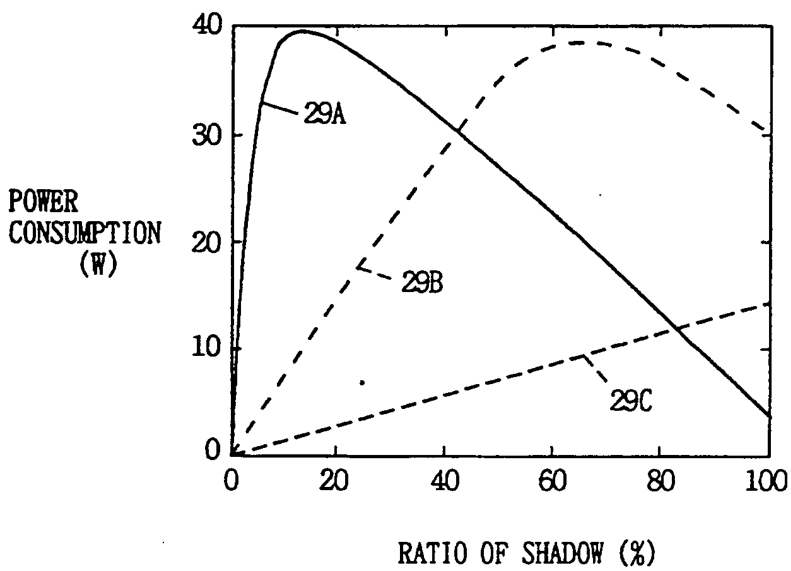

(A)
4
3
2
1
0
I (A)
28A
28C
28B
-20
-10
0
10
20
V (V)
(B)
4
3
2
1
0
I (A)
28A
28E
28D
-20
-10
0
10
20
V (V)

FIG. 29



POWER CONSUMPTION (W)
40
30
20
10
0
0
20
40
60
80
100
RATIO OF SHADOW (%)
29A
29B
29C

FIG. 30

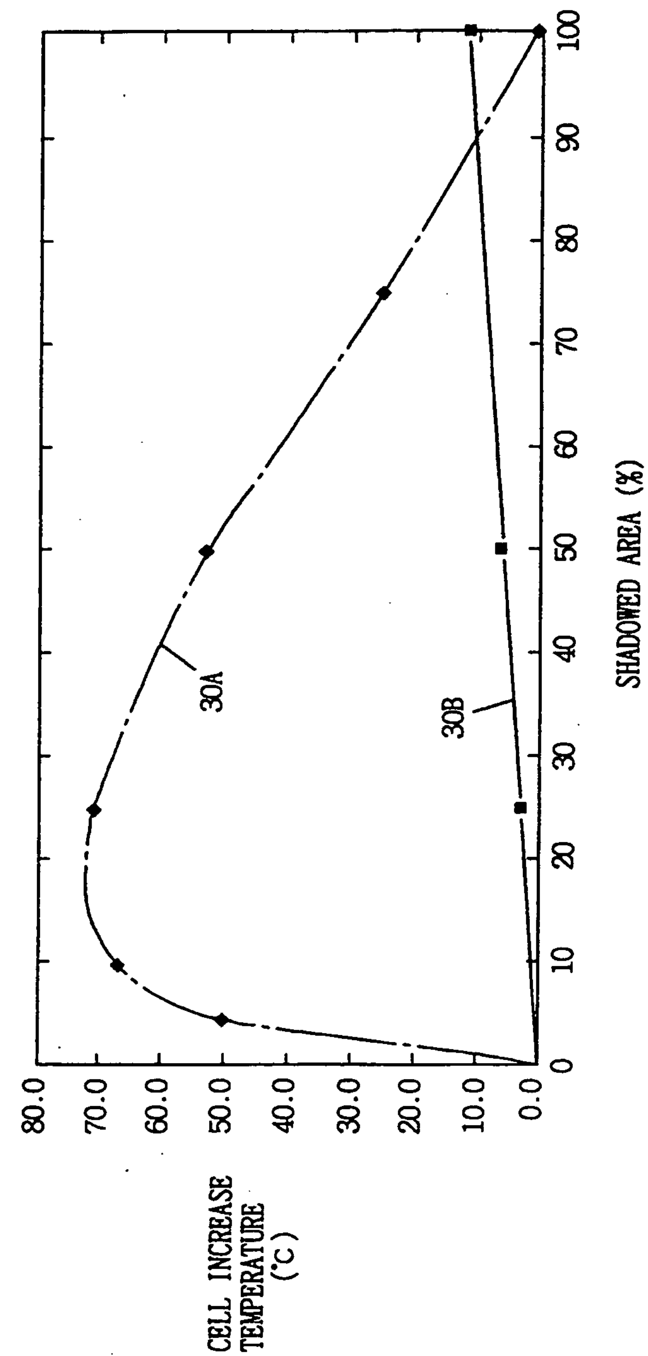

CELL INCREASE
TEMPERATURE
(°C)
80.0
70.0
60.0
50.0
40.0
30.0
20.0
10.0
0.0
0
10
20
30
40
50
60
70
80
90
100
SHADOWED AREA (%)
30A
30B

FIG. 31